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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,415	12/15/2003	Rajiv V. Joshi	YOR920030497US1	3951

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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/736,415	JOSHI ET AL.	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,14-19 and 24-35* is/are rejected.

7)☒ Claim(s) *10-13 and 20-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

DETAILED ACTION

1. Claims 1-35 are pending in the application.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description:

Fig. 2C shows a reference numeral "115" at the input of 186; however, the specification, in lines 3-4 of page 9, recites "172" as the input of 186.

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. Claims 1, 10, 20, 29 and 35 are objected to because of the following informalities:

Claim 1 recites "said write select pulses" which lacks an antecedent basis. It will be understood as --write select pulses-- in view of Fig. 1B.

Claims 10 and 20 recite "said enable node" in line 11 in each claim, which lack an antecedent basis. In view of Fig. 2A, it will be understood as --said common source node--.

Claim 29 depends on claim 27, which appears to be in error due to "said SRAM cells" lacking an antecedent basis. It will be understood to depend on claim 28.

Claim 35 depends on claim 30, which appears to be in error. It will be understood to depend on claim 31.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Raatz et al. (U.S. Pat. No. 5,546,355).

Raatz, for example in Figs. 1-3, discloses a write select circuit comprising: a pulse stretcher (50 in Fig. 2) stretching clock pulses (K; see T1 in Fig. 3; also column 2, lines 3-7); a READ/WRITE decode (the logic of 52 and 54) selectively passing stretched said clock pulses (KW) responsive to a write select signal (the combination of CS and W*); and a write driver (the output driver of 54) receiving passed said stretched clock pulses and driving write select pulses (CSWE) responsive to received said stretched clock pulses;

wherein said write select circuit is a CMOS write select circuit (see Fig. 4 showing a CMOS circuit) and said pulse stretcher comprises: a delay (D1) receiving a local clock (K) and passing a delayed clock (100); and a NAND gate (60) receiving said local clock (K) and said delayed clock (100) and providing stretched said clock pulses (via 64 and 66);

wherein said NAND gate is a 2 input NAND gate (60) and said delay is a group of series connected inverters (70-81 in Fig. 4).

6. Claims 7-9 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Kosugi et al. (U.S. Pat. No. 5,666,324).

Regarding claims 7-9, Kosugi, for example in Figs. 5, 6, 10 and 12, discloses a bit decoder comprising: a pulse stretcher (7) stretching clock pulses (CLK; see also column 16, lines 15-22); a bit decode (including 10) selectively passing stretched said clock pulses (P2) responsive to a column address (AY); and a column driver (to drive CSL) receiving passed said stretched clock pulses (P2) and driving said column select pulses (CSL) responsive to received said stretched clock pulses (P2; see Fig. 12);

wherein said bit decoder is a CMOS (see for example Fig. 10) bit decoder and said pulse stretcher comprises: a delay (D1 in Fig. 6) receiving a local clock (CLK) and passing a delayed clock (the output of 7-2); and a NAND gate (7-3) receiving said local clock and said delayed clock and providing stretched said clock pulses (via 7-5);

wherein said NAND gate is a 2 input NAND gate (7-3) and said delay is a group of series connected inverters (see, as a reference, column 12, lines 19-28).

Regarding claim 14, Kosugi, for example in Figs. 5, 6, 10 and 12, discloses a random access memory (RAM) comprising: a memory array (MA in Fig. 5) comprising a plurality of memory cells (13) organized as a plurality of rows and columns; a word decoder (8) selecting a word line identifying one of said rows responsive to a memory location access request; a bit decoder (including 10) providing column select pulses (CSL) responsive to said memory location access request; a column select (including 10 and 7) selecting a column responsive to said column select pulses (via 11 in Figs. 5 and 10); and a write select (including 6) selectively providing write select pulses (R/ZW), said write select pulses being wider than corresponding said column select pulses (see Fig. 12 showing R/WZ wider than CSL during a write operation).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Raatz et al. (U.S. Pat. No. 5,546,355) in view of Mazda (Electronics Engineer's Reference Book, 5th Edition, Butterworths, 1983, p. 30/6).

Raatz discloses a write select circuit as in claim 1, and that said write select circuit is a CMOS write select circuit (see Fig. 4), with the exception of said READ/WRITE decode being a dynamic decode comprising: a pair of series connected complementary field effect transistors (FETs), stretched said clock pulses being connected to the gates of said pair, a common drain

connection of said pair being a READ/WRITE decode output; and at least one write enable FET, selectively providing a path to ground for said pair.

Mazda, for example in Fig. 30.7(b), discloses a well-known conventional CMOS NAND gate comprising a pair of series connected complementary field effect transistors (FETs) (TR3 and TR2), an input signal (A) connected to the gates of said pair, a common drain connection of said pair being an output (C); and at least one enable FET (TR1), selectively providing a path to ground for said pair (controlled by B).

Since Mazda's CMOS NAND gate configuration was well known in the art, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to use the Mazda's CMOS NAND gate configuration for the write select circuit of Raatz (for example, for 52 in Fig. 2), such that the stretched said clock pulses are connected to the gates of the series connected FETs and the write select signal is connected to the enable FET.

9. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raatz et al. (U.S. Pat. No. 5,546,355) in view of Mazda (Electronics Engineer's Reference Book, 5th Edition, Butterworths, 1983, p. 30/6) as applied to claim 4 above, and further in view of Phillips et al. (U.S. Pat. No. 5,221,865).

The above Raatz/Mazda combination discloses a write select circuit as in claim 4, with the exception of said write driver comprising: a pseudo latch P-type FET (PFET), said READ/WRITE decode output being connected to a conductive terminal of said pseudo latch PFET; a first inverter, said READ/WRITE decode output being an input to said first inverter; and

a second inverter driving said write select pulses, an output of said first inverter being an input of said second inverter.

Phillips, for example in Fig. 5, discloses a control circuit comprising a pseudo latch P-type FET (PFET) (153), a signal being connected to a conductive terminal of said pseudo latch PFET (see Fig. 5); a first inverter (152), the signal being an input to said first inverter (see Fig. 5); and a second inverter (151) driving another signal (X), an output of said first inverter being an input of said second inverter (see Fig. 5).

Since half-latches (or pseudo latches) were common and well known in the art (as exemplified in Phillips), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate the half latch of Phillips in the write driver of the Raatz/Mazda combination, such that the decode output of Raatz is connected to the input of the first inverter and the output of the second inverter drives the write select pulses, for the purpose of increasing the switching speed of the write select pulses (see for example Phillips, column 15, lines 35-41).

10. Claims 15, 19, 24-28 and 30-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kosugi et al. (U.S. Pat. No. 5,666,324) in view of Raatz et al. (U.S. Pat. No. 5,546,355).

Kosugi discloses a RAM as in claim 15 and a bit decoder as in claims 7-9 above; and further discloses that said column select pulses (CSL) are wider than word line pulses (WL) provided to said selected word line by said word decoder (see Fig. 12); and that said plurality of memory cells are static RAM (SRAM) cells (13 in Fig. 10) or that said RAM is an SRAM macro

on an integrated circuit (IC) chip (inherent, since an SRAM, as a macro unit, is included on an IC chip).

However, Kosugi does not disclose that said write select comprises a pulse stretcher stretching clock pulses; a READ/WRITE decode selectively passing stretched said clock pulses responsive to a write select signal; and a write driver receiving passed said stretched clock pulses and driving said write select pulses responsive to received said stretched clock pulses;

wherein said pulse stretcher comprises: a delay receiving a local clock and passing a delayed clock; and a NAND gate receiving said local clock and said delayed clock and providing stretched said clock pulses;

wherein said NAND gate is a 2 input NAND gate and said delay is a group of series connected inverters;

and that said delay in said write select is twice as long as said delay in said bit decoder.

Raatz, for example in Figs. 1-3, discloses a write select circuit comprising: a pulse stretcher (50 in Fig. 2) stretching clock pulses (K; see T1 in Fig. 3; also column 2, lines 3-7); a READ/WRITE decode (the logic of 52 and 54) selectively passing stretched said clock pulses (KW) responsive to a write select signal (the combination of CS and W*); and a write driver (the output driver of 54) receiving passed said stretched clock pulses and driving write select pulses (CSWE) responsive to received said stretched clock pulses;

wherein said pulse stretcher comprises: a delay (D1) receiving a local clock (K) and passing a delayed clock (100); and a NAND gate (60) receiving said local clock (K) and said delayed clock (100) and providing stretched said clock pulses (via 64 and 66);

wherein said NAND gate is a 2 input NAND gate (60) and said delay is a group of series connected inverters (70-81 in Fig. 4).

Since both Kosugi and Raatz disclose a synchronous SRAM, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate the write select circuit of Raatz in the SRAM of Kosugi, for the purpose of reliably and consistently generating optimum write pulses and minimizing data write errors due to fluctuations in the clock frequency or duty cycle (see for example Raatz, column 1, lines 52-55 and column 2, lines 3-7).

Further, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have the delay in said write select to be twice as long as the delay in said bit decoder, since it has been held that "where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation" (i.e., discovering the optimum or workable ranges involves only routine skill in the art). *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

11. Claims 29 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kosugi et al. (U.S. Pat. No. 5,666,324) in view of Raatz et al. (U.S. Pat. No. 5,546,355) as applied to claims 28 and 31 above, and further in view of Bowers et al. (U.S. Pat. No. 4,541,076).

The above Kosugi/Raatz combination discloses a RAM as in claim 28, or a CMOS IC as in claim 31, with the exception of said SRAM cells being 2 port SRAM cells.

Bowers, for example in Fig. 9, discloses 2-port SRAM cells.

Since multi-port SRAMs, including 2-port SRAMs, were common and well known in the art (as exemplified in Bowers), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate the timing means of the above Kosugi/Raatz combination in 2-port SRAMs, for the purpose of minimizing data write errors due to fluctuations in the clock frequency or duty cycle (see for example Raatz, column 1, lines 52-55 and column 2, lines 3-7) and reducing current consumption, as well as providing reliable write operations (see for example Kosugi, column 8, lines 28-31 and column 16, lines 2-3) in 2-port SRAMs.

12. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable Kosugi et al. (U.S. Pat. No. 5,666,324) in view of Raatz et al. (U.S. Pat. No. 5,546,355) as applied to claim 15 above, and further in view of Mazda (Electronics Engineer's Reference Book, 5th Edition, Butterworths, 1983, p. 30/6).

The above Kosugi/Raatz combination discloses a write select circuit as in claim 16, and that said write select circuit is a CMOS write select circuit (see Raatz, Fig. 4), with the exception of said READ/WRITE decode is a dynamic decode comprising: a pair of series connected complementary field effect transistors (FETs), stretched said clock pulses being connected to the gates of said pair, a common drain connection of said pair being a READ/WRITE decode output; and at least one write enable FET, selectively providing a path to ground for said pair.

Mazda, for example in Fig. 30.7(b), discloses a well-known conventional CMOS NAND gate comprising a pair of series connected complementary field effect transistors (FETs) (TR3 and TR2), an input signal (A) connected to the gates of said pair, a common drain connection of

said pair being an output (C); and at least one enable FET (TR1), selectively providing a path to ground for said pair (controlled by B).

Since Mazda's CMOS NAND gate configuration was well known in the art, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to use the Mazda's CMOS NAND gate configuration for the write select circuit of Raatz (for example, for 52 in Fig. 2), such that the stretched said clock pulses are connected to the gates of the series connected FETs and the write select signal is connected to the enable FET.

13. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kosugi et al. (U.S. Pat. No. 5,666,324) in view of Raatz et al. (U.S. Pat. No. 5,546,355) and Mazda (Electronics Engineer's Reference Book, 5th Edition, Butterworths, 1983, p. 30/6) as applied to claim 16 above, and further in view of Phillips et al. (U.S. Pat. No. 5,221,865).

The above Kosugi/Raatz/Mazda combination discloses a write select circuit as in claim 16, with the exception of said write driver comprising: a pseudo latch P-type FET (PFET), said READ/WRITE decode output being connected to a conductive terminal of said pseudo latch PFET; a first inverter, said READ/WRITE decode output being an input to said first inverter; and a second inverter driving said write select pulses, an output of said first inverter being an input of said second inverter.

Phillips, for example in Fig. 5, discloses a control circuit comprising a pseudo latch P-type FET (PFET) (153), a signal being connected to a conductive terminal of said pseudo latch PFET (see Fig. 5); a first inverter (152), the signal being an input to said first inverter (see Fig.

5); and a second inverter (151) driving another signal (X), an output of said first inverter being an input of said second inverter (see Fig. 5).

Since half-latches (or pseudo latches) were common and well known in the art (as exemplified in Phillips), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate the half latch of Phillips in the write driver of the Raatz/Mazda combination, such that the decode output of Raatz is connected to the input of the first inverter and the output of the second inverter drives the write select pulses, for the purpose of increasing the switching speed for the write select pulses (see for example Phillips, column 15, lines 35-41).

Allowable Subject Matter

14. Claims 10-13 and 20-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 10 and 20, the prior arts of record do not disclose or suggest a bit decoder as recited in claim 10 or 20, and particularly, the specific arrangement of FETs for a dynamic decode which comprises the bit decoder.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Pantelakis et al. (U.S. Pat. No. 5,777,935), Yukutake et al. (U.S. Pat. No. 5,920,510) and Hori et al. (U.S. Pat. No. 6,130,846) disclose synchronous SRAMs.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7/25/05

Jung (John) Hur
Patent Examiner
Art Unit 2824

jhh